

1 1. A method, comprising:

2 disposing two rectangular diffusions of P (+) material in an n-well
3 formed in a p-substrate using a complementary metal oxide semiconductor (CMOS)
4 process;

5 disposing a polycide gate between the two rectangular diffusions of P
6 (+) material;

7 disposing a pair of inductors on the substrate; and

8 coupling the two rectangular diffusions of P (+) material and the pair of
9 inductors in a voltage-controlled oscillator (VCO) configuration.

1 2. The method of claim 1 wherein disposing two rectangular diffusions of P (+)
2 material in an n-well formed in a p-substrate using the CMOS process comprises
3 disposing two rectangular diffusions of P (+) material in an n-well formed in an
4 epitaxial substrate using the CMOS process.

1 3. The method of claim 1 wherein disposing two rectangular diffusions of P (+)
2 material in an n-well formed in a p-substrate using the CMOS process comprises
3 disposing two rectangular diffusions of P (+) material in an n-well formed in a non-
4 epitaxial substrate using the CMOS process.

1 4. The method of claim 3 wherein disposing two rectangular diffusions of P (+)
2 material in an n-well formed in a p-substrate using the CMOS process comprises
3 disposing two rectangular diffusions of P (+) material in an n-well diffused in a p-
4 substrate using the CMOS process.

1 4. The method of claim 3 wherein disposing two rectangular diffusions of P (+)
2 material in an n-well formed in a p-substrate using the CMOS process comprises
3 disposing two rectangular diffusions of P (+) material in an n-well diffused in a p-
4 substrate using the CMOS process.

1 5. The method of claim 1 wherein disposing two rectangular diffusions of P (+)
2 material in an n-well formed in a p-substrate using the CMOS process comprises
3 building a metal oxide structure on top of the n-well.

1 6. The method of claim 1 further comprising defining the spacing between the
2 two rectangular diffusions of P (+) material using a lightly doped drain (LDD)
3 structure .

1 7. The method of claim 1 further comprising defining the spacing between the
2 two rectangular diffusions of P (+) material using halo implantation.

1 8. A method, comprising:
2 forming two rectangular diffusions of P (+) material in or on an n-well
3 formed in or on a substrate; and
4 defining a spacing between the two rectangular diffusions of P (+)
5 material using a polycide gate in a complementary metal oxide semiconductor
6 (CMOS) process.

1 9. The method of claim 8, further comprising diffusing an n-well into the
2 substrate.

1 10. The method of claim 9, further comprising diffusing an N (+) well into the n-
2 well.

1 11. The method of claim 8, further comprising defining a spacing between the two
2 rectangular diffusions of P (+) material using at least one of a lightly doped drain
3 (LDD) structure or halo implantation.

1 12. The method of claim 8 wherein forming two rectangular diffusions of P (+)
2 material in or on an n-well formed in or on a substrate in a CMOS process comprises
3 forming two rectangular diffusions of P (+) material in or on an n-well formed in or
4 on a non-epitaxial substrate.

1 13. An apparatus, comprising:
2 two rectangular diffusions of P (+) material disposed in an n-well
3 diffused into a p-substrate; and
4 a polycide gate disposed between the two rectangular diffusions of P (+) material in a
5 complementary metal oxide semiconductor (CMOS) process.

1 14. The apparatus of claim 13 wherein the substrate comprises a non-epitaxial
2 substrate.

1 15. The apparatus of claim 14, further comprising a lightly doped drain (LDD)
2 disposed between the two rectangular diffusions of P (+) material.

1 16. The apparatus of claim 14, further comprising a halo implant disposed between
2 the two rectangular diffusions of P (+) material.

1 17. An article of manufacture, comprising:

2 machine-readable medium having machine-readable instructions stored
3 thereon to instruct a processor to form two rectangular diffusions of P (+) material in
4 or on an n-well formed in or on a substrate and to define a spacing between the two
5 rectangular diffusions of P (+) material using a polycide gate in a complementary
6 metal oxide semiconductor (CMOS) process.

1 18. The article of manufacture of claim 17, wherein the machine-readable
2 instructions are further to instruct the processor to diffuse an n-well into the substrate.

1 19. The article of manufacture of claim 18, wherein the machine-readable
2 instructions are further to instruct the processor to diffuse an N (+) well into the n-
3 well.

1 20. The article of manufacture of claim 17, wherein the machine-readable
2 instructions are further to instruct the processor to define a spacing between the two
3 rectangular diffusions of P (+) material using at least one of a lightly doped drain
4 (LDD) structure or halo implantation.

1 21. A system, comprising:

2 a voltage variable capacitor having two rectangular diffusions of P (+)
3 material disposed in an n-well diffused into a p-substrate and a polycide gate disposed
4 between the two rectangular diffusions of P (+) material in a complementary metal
5 oxide semiconductor (CMOS) process; and

6 a pair of inductors formed on the substrate in the CMOS process and
7 coupled to the voltage variable capacitor in a voltage-controlled oscillator (VCO)
8 configuration.

1 26. The system of claim 25 further comprising a buffer coupled to an output of the
2 loop filter and to the input of the VCO.